

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A method of transferring bursts of
2 data between a processor device and a FIFO device, said transfer
3 comprising:

4 triggering a burst transfer at the processor from a change
5 of state of a FIFO output signal by the FIFO device, said change
6 of state being an occurrence of a triggering event within the
7 FIFO device; and

8 inhibiting the FIFO device from changing state of the FIFO
9 output signal thereby inhibiting of triggering of any further
10 burst transfers until a current burst transfer is complete
11 including

12 the processor device supplying to the FIFO device an
13 end of burst signal upon completion of a burst transfer, and
14 inhibiting the FIFO device from changing state of the
15 FIFO output signal until receipt of said end of burst
16 signal.

1 2. (Original) The method of claim 1, wherein:
2 said triggering event is change in a FIFO fullness indicator
3 flag.

1 3. (Original) The method of claim 2, wherein:
2 said FIFO fullness indicator flag denotes the FIFO is less
3 than or greater than half full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting less than half full to greater than half
6 full.

1 4. (Original) The method of claim 2, wherein:
2 said fullness indicator denotes less than or greater than
3 half full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting greater than half full to less than half
6 full.

1 5. (Original) The method of claim 1, wherein:
2 said burst transfer includes transfer of predetermined
3 amount of data in fixed number of sequential clock cycles.

6 to 10. (Canceled)

1 11. (Currently Amended) ~~The A~~ method of ~~claim 1, wherein~~
2 transferring bursts of data between a processor device and a FIFO
3 device, said transfer comprising:

4 triggering a burst transfer at the processor from a change
5 of state of a FIFO output signal by the FIFO device, said change
6 of state being an occurrence of a triggering event within the
7 FIFO device; and

8 ~~said step of~~ inhibiting the FIFO device from changing state
9 of the FIFO output ~~signal, signal~~ thereby inhibiting further
10 burst transfers ~~includes~~ until a current burst transfer is
11 complete including

12 the FIFO device counting a predetermined number of
13 cycles corresponding to a burst transfer size, and

14 inhibiting the FIFO device from changing state of the
15 FIFO output signal until completion of counting the
16 predetermined number of cycles.

1 12. (New) The method of claim 11, wherein:
2 said triggering event is change in a FIFO fullness indicator
3 flag.

1 13. (New) The method of claim 12, wherein:
2 said FIFO fullness indicator flag denotes the FIFO is less
3 than or greater than half full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting less than half full to greater than half
6 full.

1 14. (New) The method of claim 12, wherein:
2 said fullness indicator denotes less than or greater than
3 half full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting greater than half full to less than half
6 full.

1 15. (New) The method of claim 11, wherein:
2 said burst transfer includes transfer of predetermined
3 amount of data in fixed number of sequential clock cycles.